Lab 7

JFET Biasing

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Objective

- Investigate the JFET self-bias configuration.
- Investigate the JFET voltage-divider bias configuration.
- Calculate JFET dc q-points for each bias configuration

Results

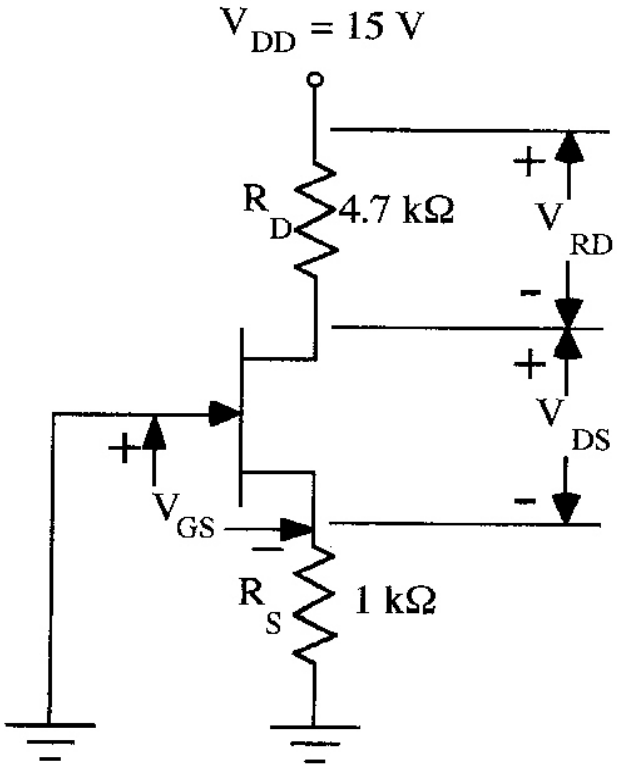

Figure 3

Idss and Vp for the JFET must be calculated based on the actual transistor itself.
In doing this, I determined the values to be as follows:
Idss=6.79mA
Vp = 2.906V

Vrd = 7.27V
Vds = 6.18V
Vgs = 1.55V

Given Vgs, I was able to calculate Id = Idss(1-Vgs/Vp)^2 = 1.48mA

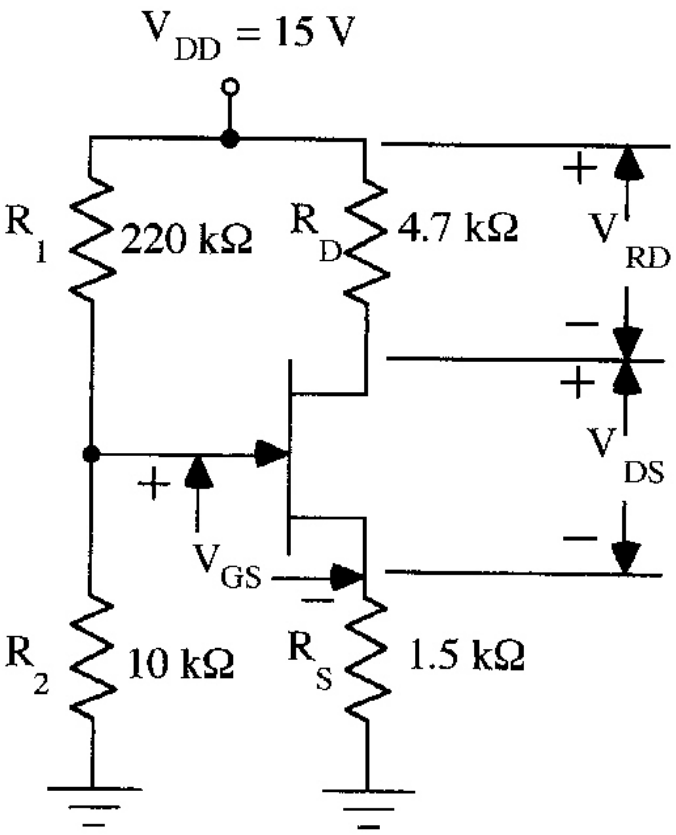

Figure 4

Vgs = 1.57V
Vds = 5.85V
Vrd = 6.92V

Id = Idss(1-Vgs/Vp)^2 = 1.44mA

Analysis
In a self-biased JFET circuit, Id=Idss when Vg=0V.
In a voltage-divider JFET circuit, the load line crosses Id=0 when Vgs > 0V, therefore Id=Idss occurs