

Lab 4  
VHDL Gates

Jeff Morrison  
CSCE 3730  
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## Description

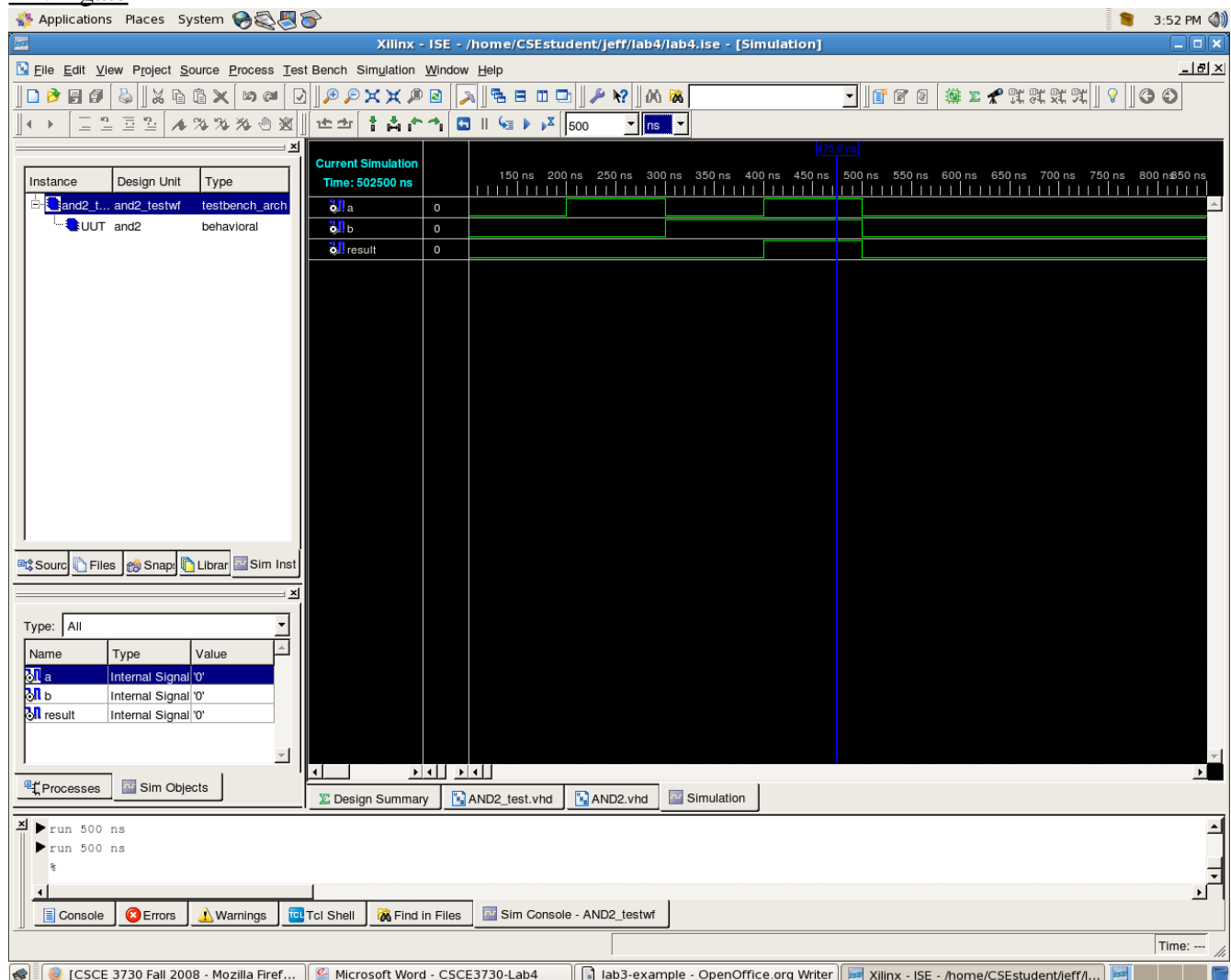
The purpose of this project was to design the fundamental logic gates and components (using VHDL modules) that will be required to create the subcomponents of our 4bit ALU semester project.

## Analysis

Each of these gates and components were fairly simple to design with minimal amounts of VHDL code per module. However, since they will be used repetitively in the overall ALU design, it is useful to have them ready to go.

## Component Test-bench Waveforms

### AND gate



# OR gate

The screenshot shows the Xilinx ISE simulation environment. The main window displays a waveform for a behavioral simulation of an OR gate. The simulation time is 1000 ns. The waveform shows three signals: 'a', 'b', and 'result'. Signal 'a' is high from 0 ns to 300 ns and low from 300 ns to 900 ns. Signal 'b' is high from 0 ns to 600 ns and low from 600 ns to 900 ns. The 'result' signal is high from 0 ns to 300 ns, low from 300 ns to 600 ns, and high from 600 ns to 900 ns, which is the correct OR gate output.

The console window at the bottom shows the following text:

```
Simulator is doing circuit initialization process.  
Finished circuit initialization process.  
*
```

# NOT gate

The screenshot displays the Xilinx ISE software interface during a behavioral simulation of a NOT gate. The main window shows a timing diagram with a signal 'a' that is high from 0 ns to 200 ns and low from 200 ns to 500 ns. The output signal 'result' is high from 0 ns to 200 ns and low from 200 ns to 500 ns, demonstrating the correct NOT gate functionality. The simulation time is 500 ns.

**Sources for: Behavioral Simulation**

- lab4
  - xc4vlx15-12sf363
    - AND2 - Behavioral (AND2.vhd)
    - OR2 - Behavioral (OR2.vhd)
    - AND2\_testwf (AND2\_testwf.tbw)
    - NOT1\_testwf (NOT1\_testwf.tbw)
    - OR2\_testwf (OR2\_testwf.tbw)

**Processes for: NOT1\_testwf**

- Add Existing Source
- Create New Source
- View Generated Test Bench As HDL
- Add Test Bench To Project
- Xilinx ISE Simulator
- Simulate Behavioral Model

**Simulation Console:**

```
Simulator is doing circuit initialization process.  
Finished circuit initialization process.  
*
```

The taskbar at the bottom shows the following open applications: [CSCE 3730 Fall 2008 - Mo...], [Microsoft Word - CSCE373...], [lab3-example - OpenOffic...], [Xilinx - ISE - /home/CSEstu...], and [lab4 - File Browser].

# Adder component

The screenshot displays the Xilinx ISE simulation environment. The main window shows a behavioral simulation of an adder component. The simulation console at the bottom indicates that the circuit initialization process is complete. The timing diagram on the right shows the signals a, b, sum, and carry over time.

**Simulation Console:**

```
Simulator is doing circuit initialization process.  
Finished circuit initialization process.  
*
```

**Timing Diagram:**

Signal	Value	Start Time (ns)	End Time (ns)
a	1	0	250
b	1	0	300
sum	0	0	500
carry	1	0	300

**Source Tree:**

- lab4
  - xc4vlx15-12sf363
    - AND2 - Behavioral (AND2.vhd)
    - OR2 - Behavioral (OR2.vhd)
    - ADDER2\_testwf (ADDER2\_testwf.tbw)
    - UUT - ADDER2 - Behavioral (ADDER2\_testwf.tbw)
    - AND2\_testwf (AND2\_testwf.tbw)
    - MULT2to1\_testwf (MULT2to1\_testwf.tbw)
    - MULT4to1\_testwf (MULT4to1\_testwf.tbw)
    - NOT1\_testwf (NOT1\_testwf.tbw)
    - OR2\_testwf (OR2\_testwf.tbw)

## 2 to 1 Multiplexer component

The screenshot displays the Xilinx ISE simulation environment. The main window shows a timing diagram for a 2-to-1 multiplexer testbench. The simulation time is 1000 ns. The signals shown are 'a', 'b', 'sel', and 'result'. The signal 'a' is high from 0 to 200 ns and low from 200 to 1000 ns. The signal 'b' is low from 0 to 400 ns and high from 400 to 1000 ns. The signal 'sel' is high from 0 to 400 ns and low from 400 to 1000 ns. The signal 'result' is high from 0 to 400 ns and low from 400 to 1000 ns. The testbench files are listed in the Sources for: Behavioral Simulation window, including AND2.vhd, OR2.vhd, ADDER2\_testwf.tbw, AND2\_testwf.tbw, MULT2to1\_testwf.tbw, NOT1\_testwf.tbw, and OR2\_testwf.tbw. The Processes for: MULT2to1\_testwf window shows the Xilinx ISE Simulator and Simulate Behavioral Model. The Console window shows the simulator initialization process.

Applications Places System 4:16 PM

Xilinx - ISE - /home/CSEstudent/jeff/lab4/lab4.Ise - [Simulation]

File Edit View Project Source Process Test Bench Simulation Window Help

Sources for: Behavioral Simulation

- lab4
  - xc4vlx15-12sf363
    - AND2 - Behavioral (AND2.vhd)
    - OR2 - Behavioral (OR2.vhd)
    - ADDER2\_testwf (ADDER2\_testwf.tbw)
    - AND2\_testwf (AND2\_testwf.tbw)
    - MULT2to1\_testwf (MULT2to1\_testwf.tbw)
    - NOT1\_testwf (NOT1\_testwf.tbw)
    - OR2\_testwf (OR2\_testwf.tbw)

Current Simulation Time: 1000 ns

Signal	0 ns	100 ns	200 ns	300 ns	400 ns	500 ns	600 ns	700 ns	800 ns	900 ns	1000 ns
a	0	0	0	0	0	0	0	0	0	0	0
b	0	0	0	0	0	0	0	0	0	0	0
sel	0	0	0	0	0	0	0	0	0	0	0
result	0	0	0	0	0	0	0	0	0	0	0

Processes for: MULT2to1\_testwf

- Add Existing Source
- Create New Source
- View Generated Test Bench As HDL
- Add Test Bench To Project
- Xilinx ISE Simulator
- Simulate Behavioral Model

Design Summary MULT2to1.vhd MULT2to1\_testwf.tbw Simulation

Simulator is doing circuit initialization process.  
Finished circuit initialization process.  
\*

Console Errors Warnings Tcl Shell Find in Files Sim Console - MULT2to1\_testwf

Time: ---

CSCE 3730 Fall 2008 - Mozilla Firefox Microsoft Word - CSCE3730-Lab4 lab3-example - OpenOffice.org Writer Xilinx - ISE - /home/CSEstudent/jeff/...

