Lab 4
VHDL Gates

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CSCE 3730
11/11/08

Description

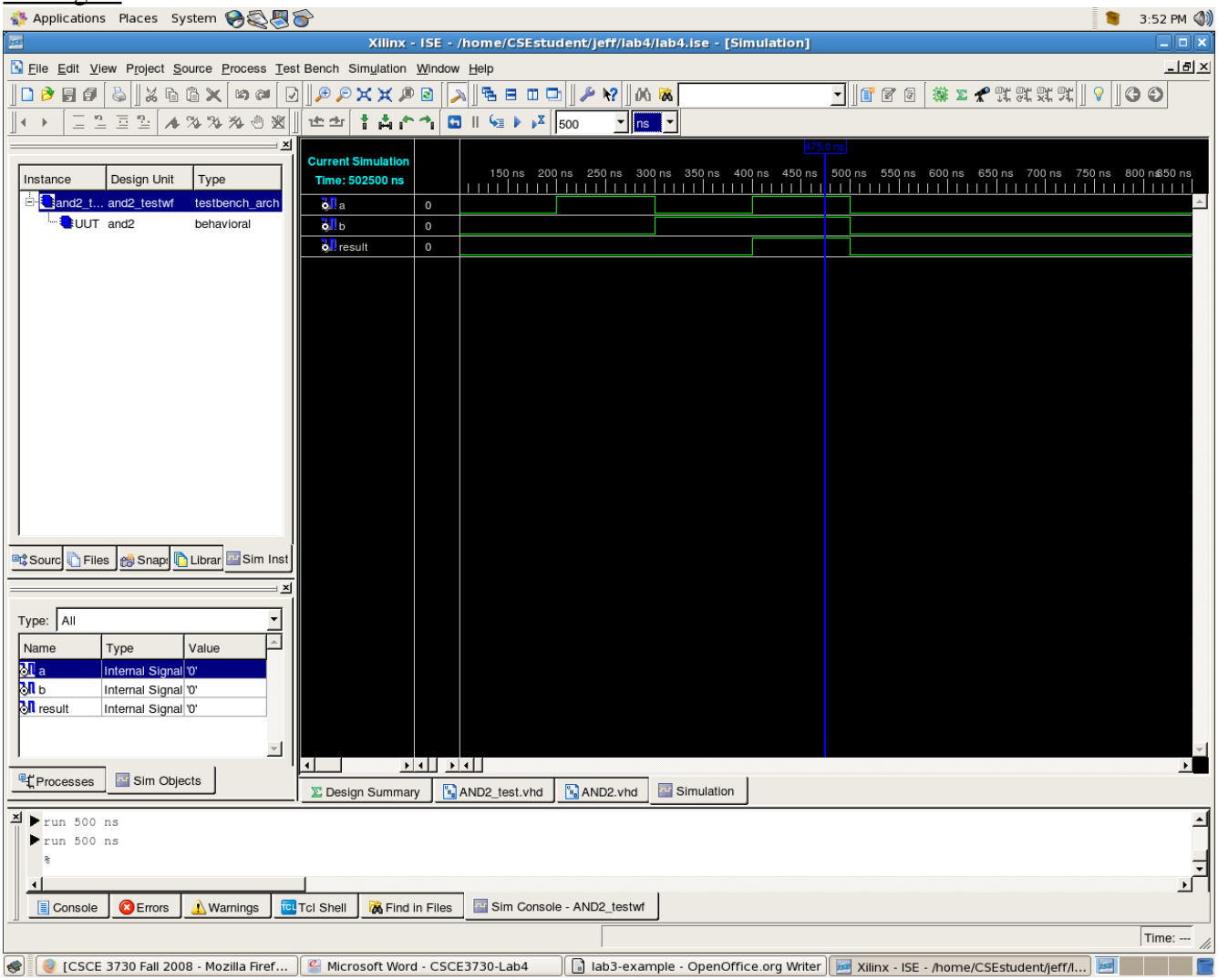
The purpose of this project was to design the fundamental logic gates and components (using VHDL modules) that will be required to create the subcomponents of our 4bit ALU semester project.

Analysis

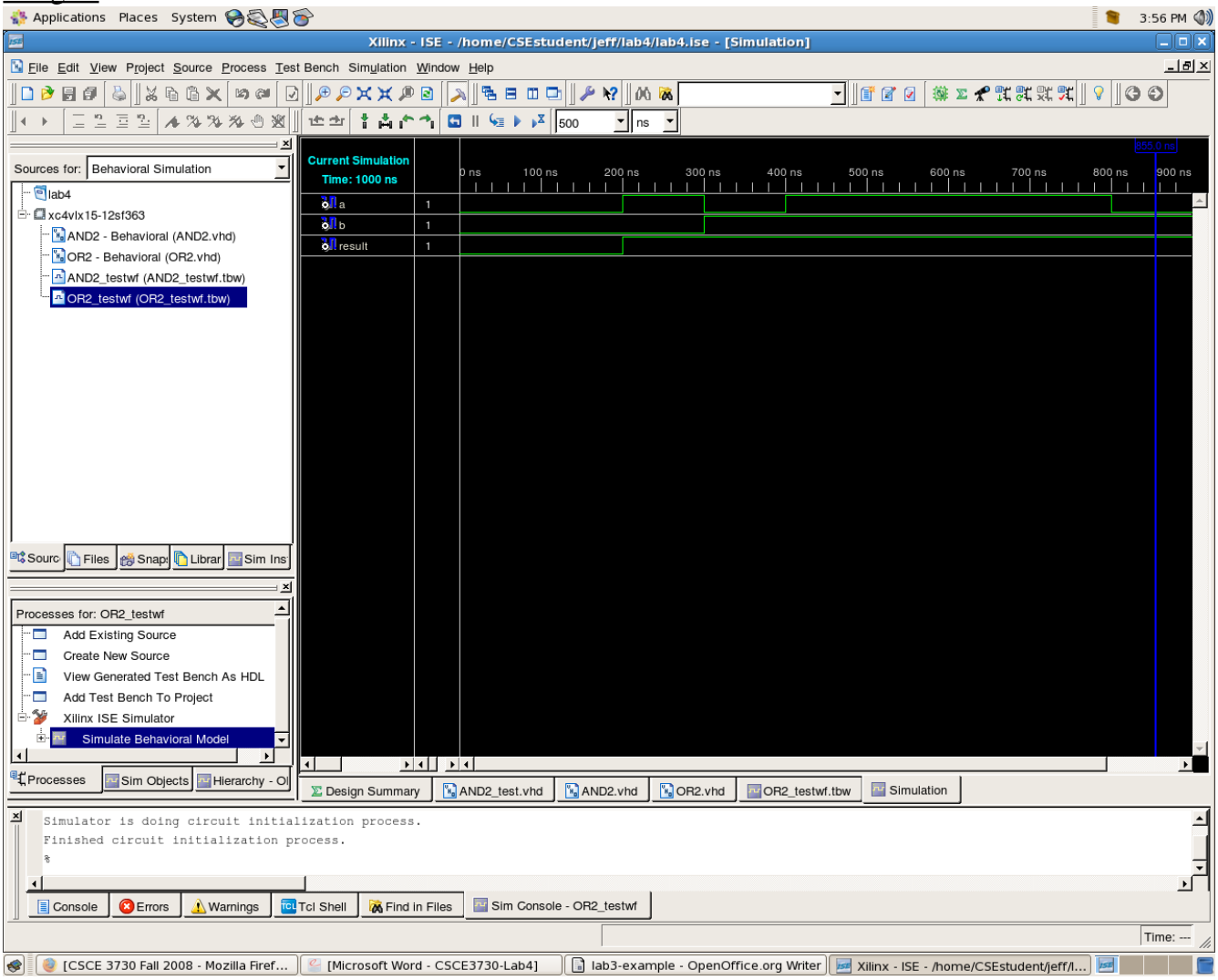
Each of these gates and components where fairly simple to design with minimal amounts of VHDL code per module. However, since they will be used repetitively in the overall ALU design, it is useful to have them ready to go.

Component Test-bench Waveforms

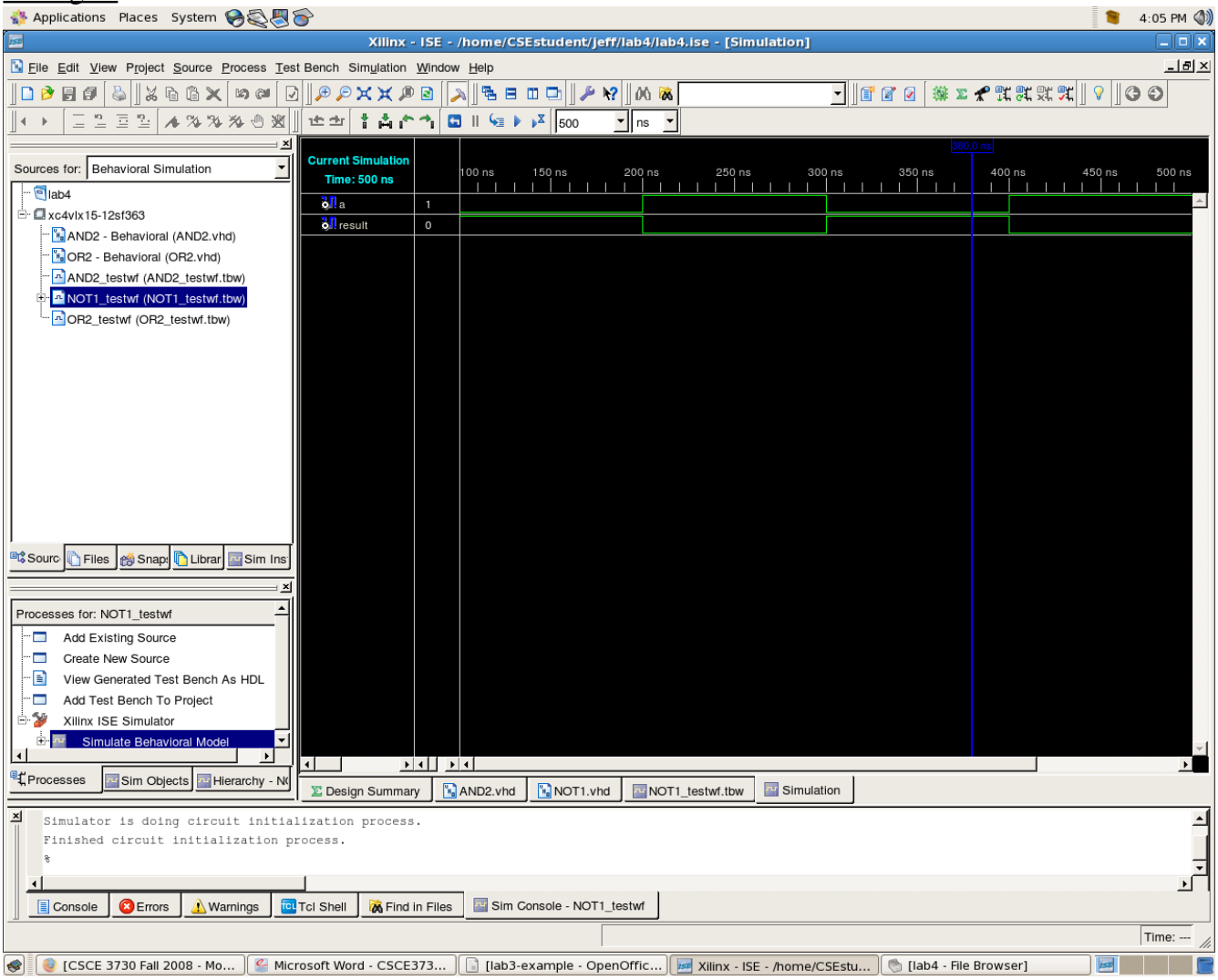
AND gate



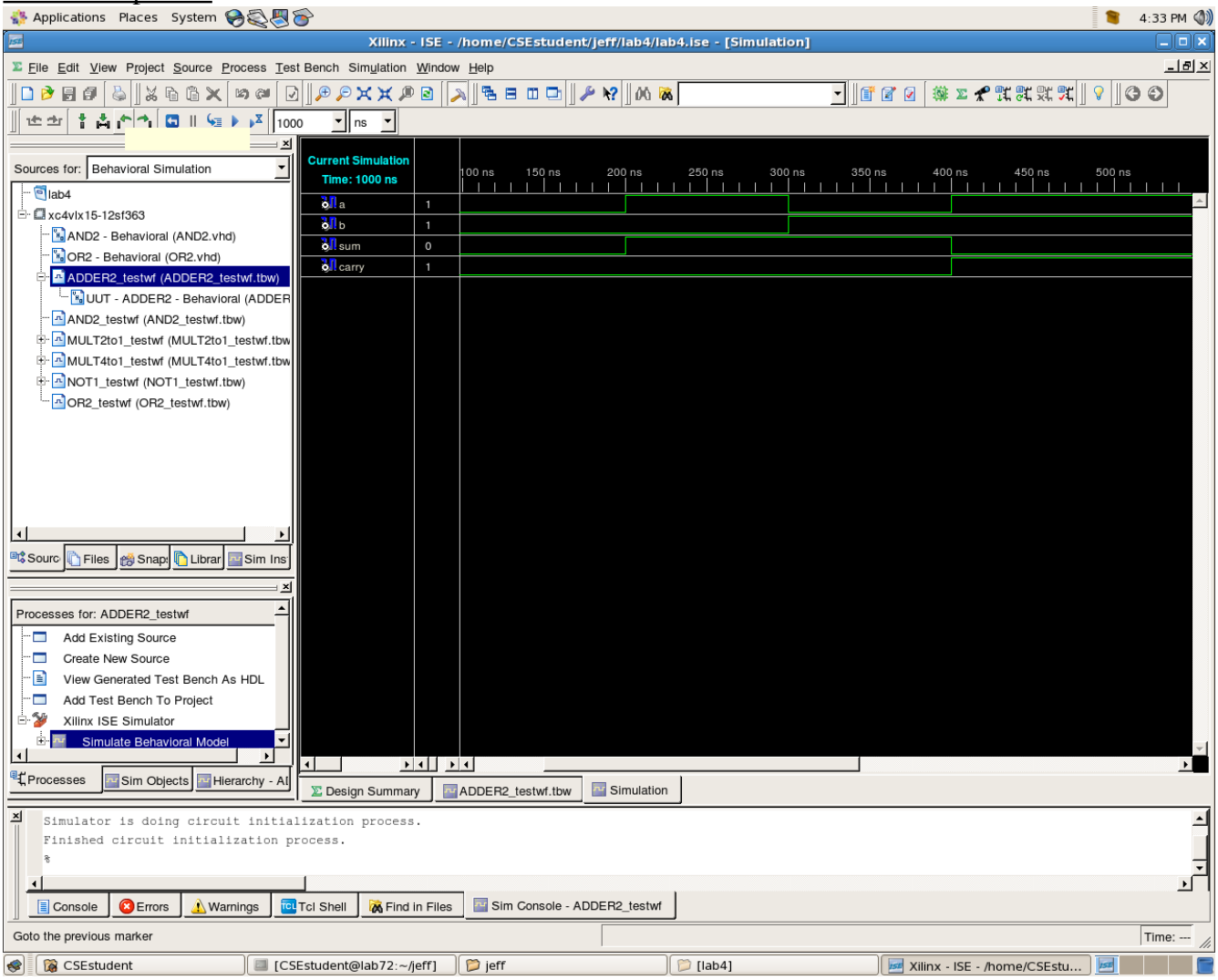
OR gate


Applications Places System
3:56 PM
Xilinx - ISE - /home/CSEstudent/jeff/lab4/lab4.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
Sources for: Behavioral Simulation
lab4
xc4vlx15-12sf363
AND2 - Behavioral (AND2.vhd)
OR2 - Behavioral (OR2.vhd)
AND2_testwf (AND2_testwf.tbw)
OR2_testwf (OR2_testwf.tbw)
Current Simulation Time: 1000 ns
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
900 ns
a
b
result
Processes for: OR2_testwf
Add Existing Source
Create New Source
View Generated Test Bench As HDL
Add Test Bench To Project
Xilinx ISE Simulator
Simulate Behavioral Model
Design Summary
AND2_test.vhd
AND2.vhd
OR2.vhd
OR2_testwf.tbw
Simulation
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Errors
Warnings
Tcl Shell
Find in Files
Sim Console - OR2_testwf
Time: ---
[CSCE 3730 Fall 2008 - Mozilla Firef...
[Microsoft Word - CSCE3730-Lab4]
lab3-example - OpenOffice.org Writer
Xilinx - ISE - /home/CSEstudent/jeff/l...

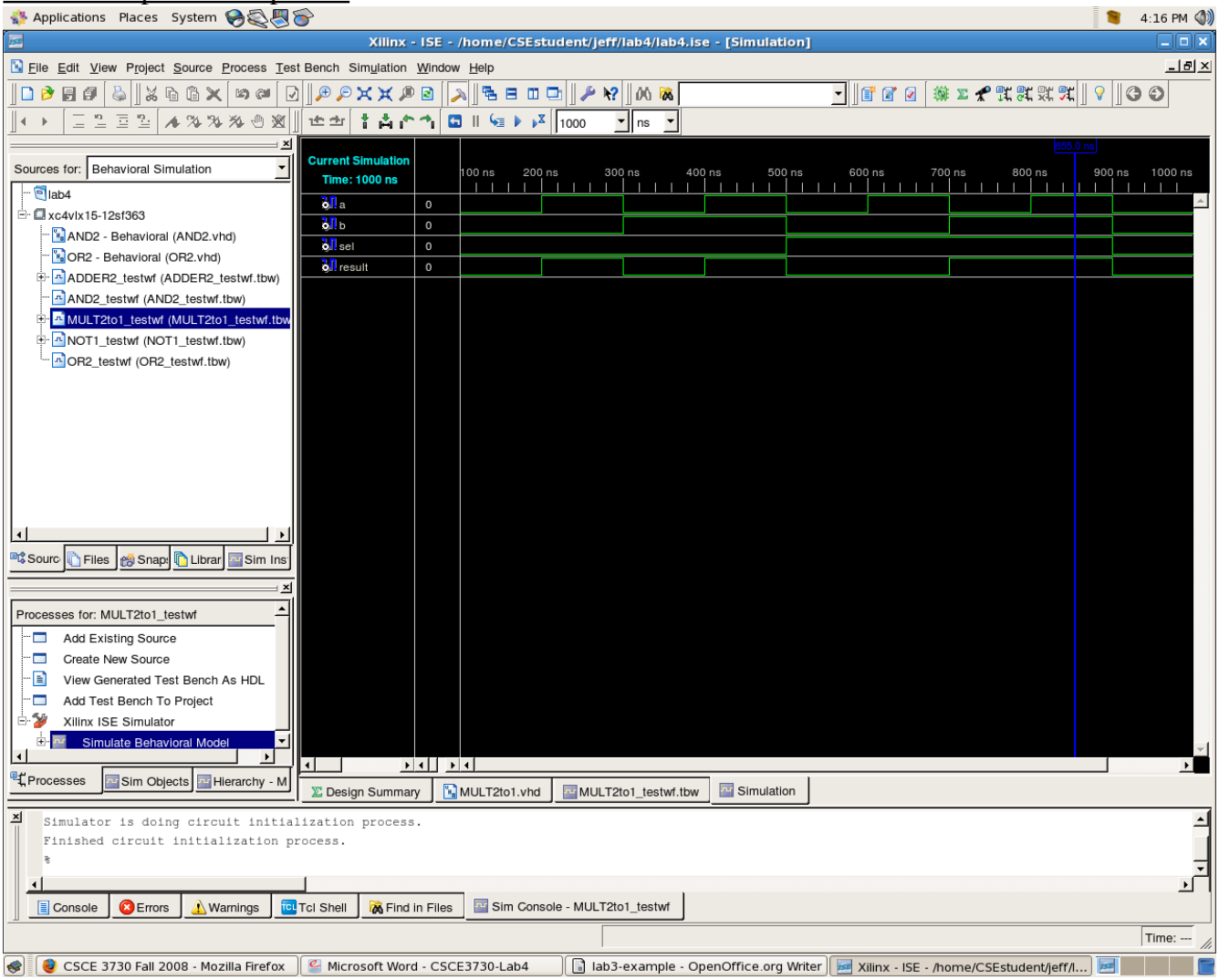
NOT gate


Applications Places System
4:05 PM
Xilinx - ISE - /home/CSEstudent/jeff/lab4/lab4.ise - [Simulation]
File Edit View Project Source Process Test Bench Simulation Window Help
Sources for: Behavioral Simulation
lab4
xc4vlx15-12sf363
AND2 - Behavioral (AND2.vhd)
OR2 - Behavioral (OR2.vhd)
AND2_testwf (AND2_testwf.tbw)
NOT1_testwf (NOT1_testwf.tbw)
OR2_testwf (OR2_testwf.tbw)
Processes for: NOT1_testwf
Add Existing Source
Create New Source
View Generated Test Bench As HDL
Add Test Bench To Project
Xilinx ISE Simulator
Simulate Behavioral Model
Current Simulation Time: 500 ns
100 ns 150 ns 200 ns 250 ns 300 ns 350 ns 400 ns 450 ns 500 ns
a
result
Design Summary
AND2.vhd
NOT1.vhd
NOT1_testwf.tbw
Simulation
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Console
Errors
Warnings
Tcl Shell
Find in Files
Sim Console - NOT1_testwf
Time:

Adder component



2 to 1 Multiplexer component



4 to 1 Multiplexer Component